Speeding Up Quantified Bit-Vector SMT Solvers by Bit-Width Reductions and Extensions

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Theory of Bit-Vectors

The theory of bit-vectors describes bounded integers (or vectors of bits of fixed size) with:

- bitwise operations,
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In many software verification applications, quantifiers are necessary. For example in

- invariant generation,
- ranking function synthesis,
- cycle summarization,
- symbolic state equality test.

Bit-with Reductions

In the formula

$$\forall x^{[32]} \exists y^{[32]} \, (x^{[32]} + y^{[32]} = 0^{[32]})$$

- $x^{[32]}$ and $y^{[32]}$ are variables of bit-width 32,
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Observation
Performance of the solvers for quantified bit-vector formulas usually depends on the bit-widths used in the formula.

Bit-width Reductions and Satisfiability

Observation from our LPAR 2018 paper
Vast majority of quantified bit-vectors does not change their satisfiability from very low bit-widths.

	Total	Different answer for some bit-width			
		≥ 1b	≥ 2b	≥ 4b	≥ 8b
Count	4905	216	95	32	14
%	100	4.4	1.9	0.65	0.29

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Challenges

- Can the safe bit-width be computed from the formula?
- Can the observation be leveraged to speed-up SMT solvers?

Outline of the Presentation

1. How to decide satisfiability using bit-width reductions
2. How to decide unsatisfiability using bit-width reductions
3. Our implementation in a single algorithm
4. Experimental evaluation

Symbolic Models of Quantified Formulas

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$$\Big\downarrow \text{ solve}$$

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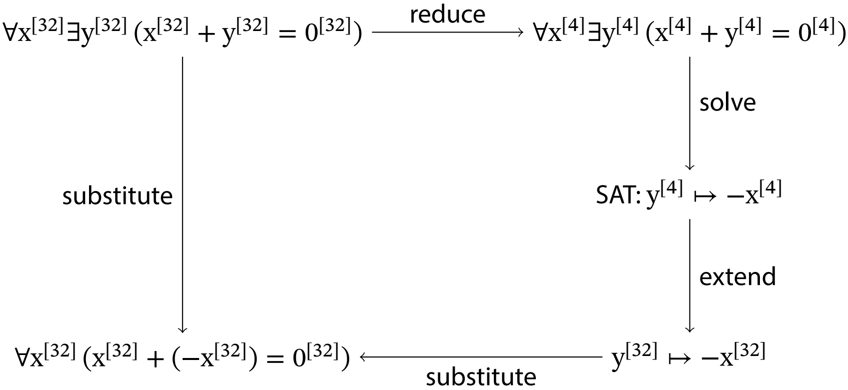
$$\Big\downarrow \text{ extend}$$

$$y^{[32]} \mapsto -x^{[32]}$$

Deciding Satisfiability With Reductions



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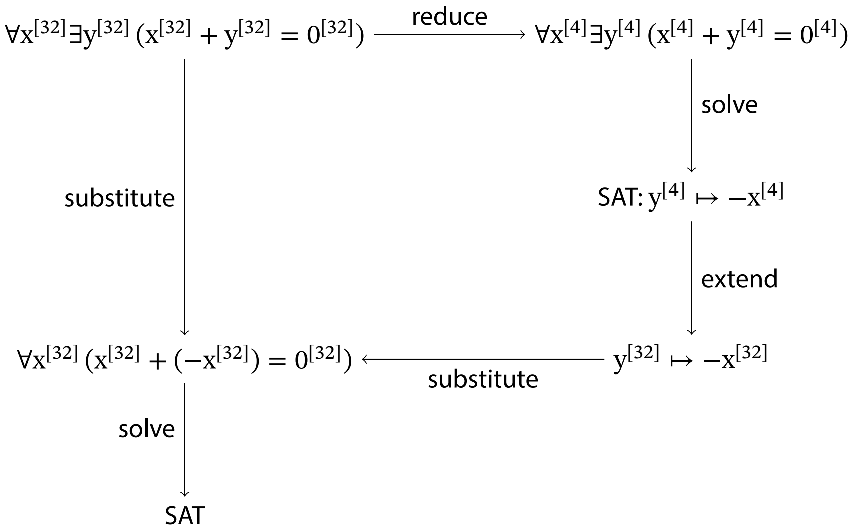

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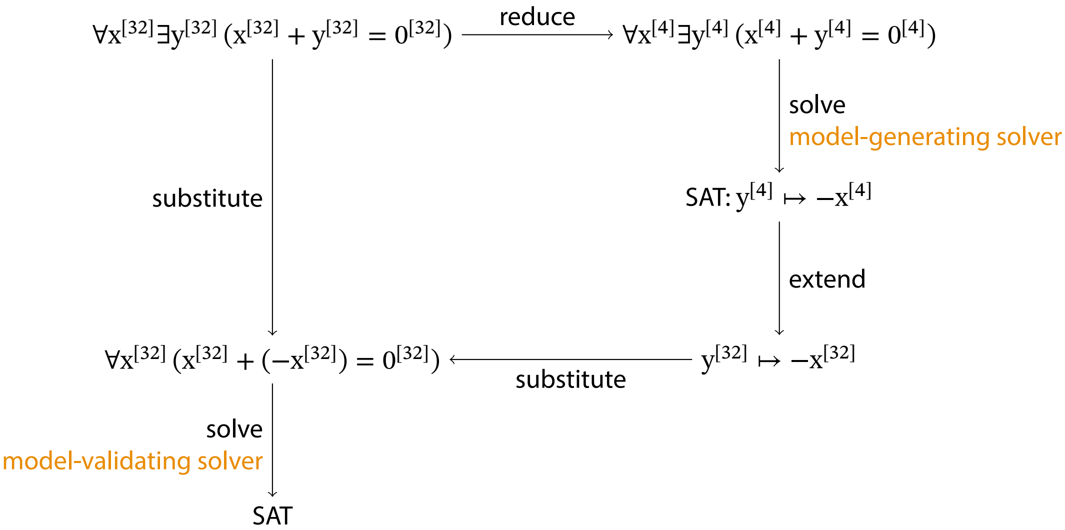

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$$x^{[32]} \mapsto -y^{[32]} + 1^{[32]}$$

because

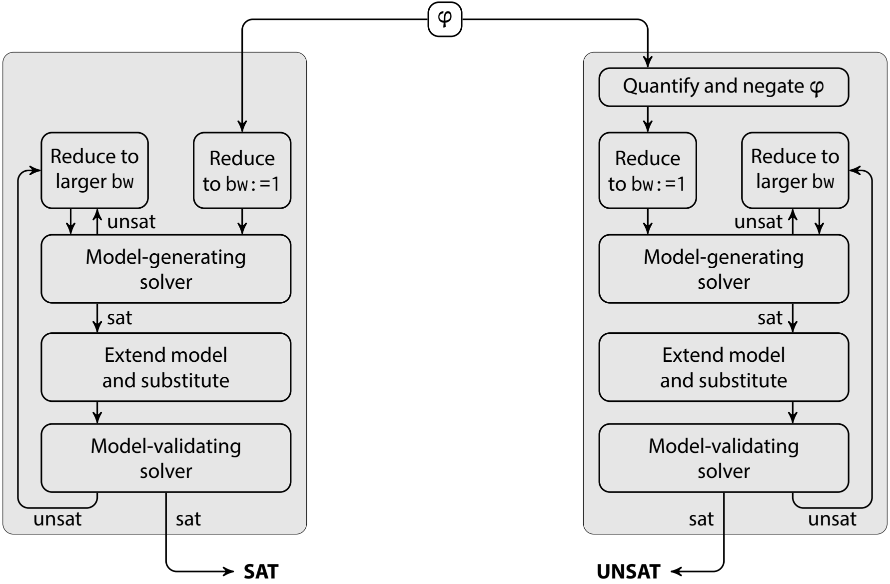
$$(-y^{[32]} + 1^{[32]}) + y^{[32]} = 0^{[32]}$$

is unsatisfiable.

Overall Algorithm

1. Reduce the formula.
2. Try to solve its satisfiability.
3. Get a symbolic model/countermodel.
4. Extend the symbolic model/countermodel to the original bit-width.
5. Check whether it is a symbolic model/countermodel of the original formula.
6. If unsuccessful, increase the reduction bit-width and repeat.

Overall Algorithm – Practical Implementation



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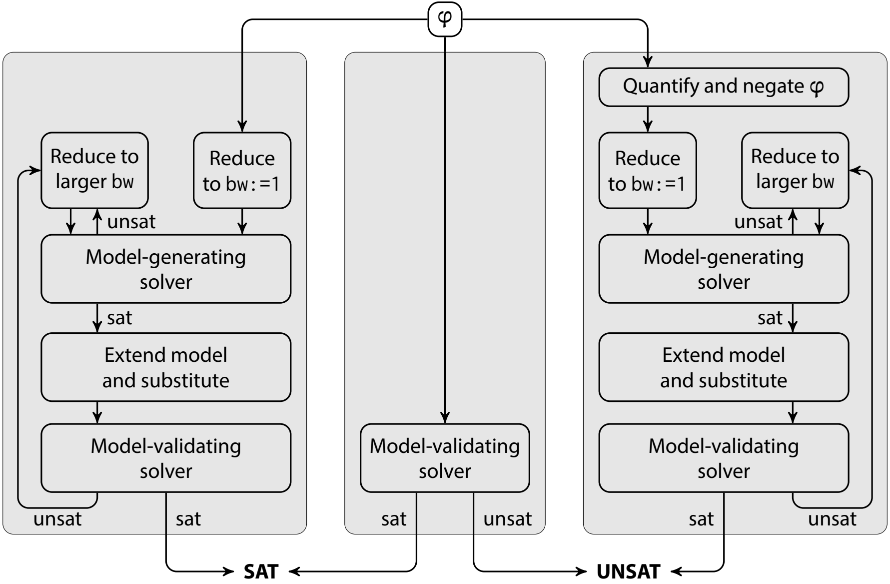

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- reductions, extensions, and the solving algorithm
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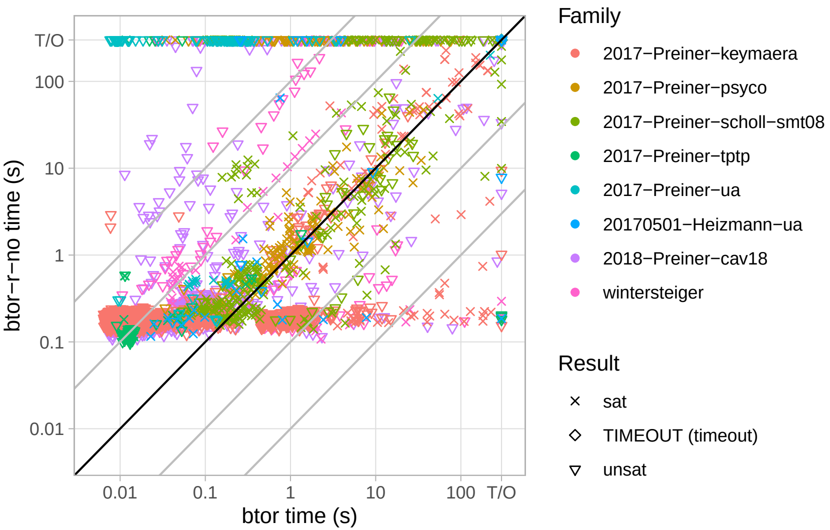
Model-validating solver

- Boolector
- CVC4
- Q3B

Effect of Reductions on Boolector



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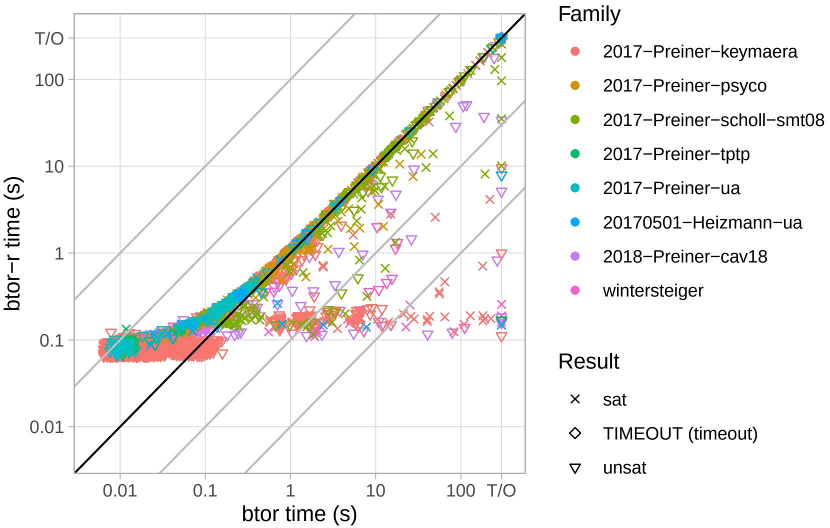


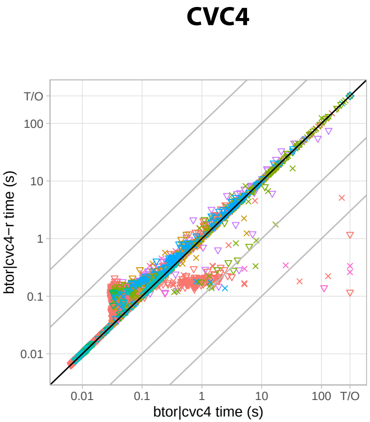
Effect of Reductions on Boolector

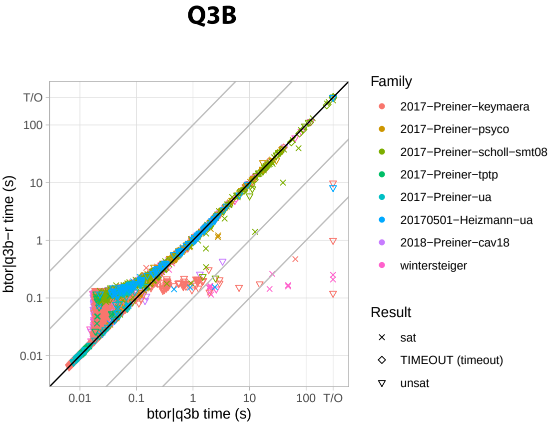
Reducing solver solved 449 formulas faster than Boolector itself.

Used bit-widths for these formulas:

Reduced bit-width	1	2	4	8	16
Count	185	119	122	17	6

Effect on CVC4 and Q3B





Newly Solved Formulas

With reductions, all the solvers were able to solve some previously unsolved formulas:

- Boolector – 22 formulas
- CVC4 – 4 formulas
- Q3B – 7 formulas

Conclusions

We have developed a technique that

- solves satisfiability of formulas with reduced bit-widths,
- extends the models/countermodels to the original bit-width,
- verifies the extended models/countermodels.

We have shown that this technique

- can improve performance of state-of-the-art SMT solvers,
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Thank you for your attention.